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Code No. : 14425

**VASAVI COLLEGE OF ENGINEERING (Autonomous), HYDERABAD**

**B.E. (E.C.E. : CBCS) IV-Semester Main Examinations, January-2021**

**Digital System Design**

Time: 2 hours

Max. Marks: 60

*Note: Answer any NINE questions from Part-A and any THREE from Part-B*

**Part-A (9 × 2 = 18 Marks)**

Q. No.	Stem of the question	M	L	CO	PO
1.	Mention any four important Boolean postulates	2	1	1	1
2.	Realize Ex-OR gate using NAND gates	2	1	1	2
3.	Differentiate between a multiplexer and Encoder operation	2	1	2	1
4.	Draw the circuit of Full Adder and write expressions for SUM and CARRY	2	1	2	1
5.	Write the properties of Pseudo random binary sequence	2	2	3	1
6.	Differentiate between a latch and flip flop	2	1	3	2
7.	Write about any two compiler directives.	2	2	4	1
8.	What is a test bench? Write its significance.	2	2	4	1
9.	Mention various timing controls used in HDLs	2	2	5	2
10.	What is logic synthesis?	2	2	5	1
11.	Minimize the 3 variable function using Boolean laws. $F(A,B,C)=\Sigma m(0,1,2,3,5,7)$	2	2	1	2
12.	Draw a schematic diagram of 4-bit subtractor using RCA and associated circuitry.	2	2	2	2
<b>Part-B (3 × 14 = 42 Marks)</b>					
13. a)	Design a BCD to 7 segment decoder and realize the circuit using NAND gates only	7	4	1	2
b)	Explain Ex-OR and Ex-NOR simplification of K-maps with suitable example	7	4	1	2
14. a)	Design BCD adder circuit and explain its operation in detail.	7	3	2	3
b)	Design a two bit magnitude comparator and explain its operation in detail.	7	3	2	3
15. a)	Explain the steps to design a synchronous counter with the given type of flip flop.	6	2	3	4
b)	Design a 4 bit shift right register. Use JK flip flops. Draw the truth table and explain it.	8	4	3	4

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16. a)	Differentiate among various styles of modeling, namely Dataflow, Behavioral and gate level in detail	6	2	4	2
b)	Write a Verilog module to implement a 4-bit binary adder using 1-bit adder. Use structural model. Write a test bench to verify your design	8	4	4	3
17. a)	Design verilog module for a mod-13 counter with synchronous clear and preset. Verify your design with a suitable test bench. Use behavioral model	8	4	5	3
b)	Write a HDL program for a sequence detector to detect 101011. Use mealy type modeling, no overlap of sequence is allowed.	6	5	5	3
18. a)	Realize the following functions of 4 variables using 8:1 Mux. (i) $F1 = \Sigma m(0,3,5,6,9,10,12,15)$ (ii) $F2 = \Sigma m(0,1,2,3,11,12,14,15)$	7	3	1	4
b)	Design an 8 bit priority encoder and explain its significance with truth table.	7	3	2	3
19.	Answer any <i>two</i> of the following:				
a)	Design a mod10 ripple counter using JK flip flops.	7	3	3	4
b)	Draw the switch level model of 2 bit EX-OR gate and write the Verilog code.	7	3	4	3
c)	Differentiate between blocking and non blocking assignment with suitable example.	7	2	5	2

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	50
2	Knowledge on application and analysis (Level-3 & 4)	45
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	05

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